Integrated Circuit

MODEL 999

I C Tester

(PREFIX 500)

Beckman

Operating and Servicing Manual

Electronic Instruments Division

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MODEL 999

I C Tester

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Beckman

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ELECTRONIC INSTRUMENTS DIVISION
RICHMOND, CALIFORNIA • 94804

OCTOBER 1967

BII No. 015-436132

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ADDENDUM A

MODEL 999

Please add the following sentence to the end of the first paragraph of Section 1.4.7, top of page 1-10:

> In EXT, the voltage swing must be from less than 0.4 volt (but not lower than -2 volts) to greater than +5 volts (but not higher than +12 volts).

ADDENDUM B

MODEL 999

Please make the following changes to the Power Supply Schematic (dwg. no. D435931):

1) Change R1 from 2.7Ω to 2.2Ω.
2) Change R8 from 2.7Ω to 1.8Ω.

MODEL 999 IC TESTER

TABLE OF CONTENTS

Paragraph Number	Description	Page No.
1.0	Introduction	1-1
1.1	Specifications	1-1
1.2	Programming and Controls	1-3
1.3	Meter Panel	1-3
1.3.1	Meter	1-3
1.3.2	Range	1-5
1.3.3	Pin Selector	1-5
1.4	Control Panel	1-5
1.4.1	Programming Matrix	1-8
1.4.2	EXT.	1-8
1.4.3	VCC 0-10V	1-9
1.4.4	VCC +12V	1-9
1.4.5	VCC +5V	1-9
1.4.6	GRD	1-9
1.4.7	CLOCK	1-9
1.4.8	VIN HI and VIN LO	1-11
1.4.9	BUSS 1 and BUSS 2	1-11
1.4.10	500 pf and 50 pf Loads	1-12
1.4.11	I SOURCE	1-12
1.4.12	I SINK	1-13
1.5	Integrated Circuits Measurements	1-14
1.5.1	Typical NAND Gate Testing	1-15
1.5.1.1	Output Low Voltage	1-15
1.5.1.2	Output High Voltage	1-17

Table Of Contents (Cont'd.)

Paragraph Number	Description	Page
1.5.1.3	Input High Voltage (Threshold Level)	1-17
1.5.1.4	Supply Current	1-17
1.5.1.5	Input Current	1-18
1.5.2	Typical Flip-Flop Testing	1-19
1.5.2.1	J-K Mode Operation (9000, Figure 1-9)	1-19
1.5.2.2	Logic Gate Operation	1-21
1.5.3	Extensive Flip-Flop Testing	1-21
1.5.3.1	J-K Mode Operation	1-23
1.5.3.2	Truth Logic	1-24
1.5.3.3	Supply Current	1-25
1.5.3.4	Input Current	1-26
1.6	Maintenance	1-26
1.6.1	Power Supply Adjustments	1-29
1.6.2	Current Source Adjustments	1-29
1.6.3	Current SINK Adjustment	1-29

LIST OF ILLUSTRATIONS

Figure Number	Description	Page
1-1	Operating Controls	1-4
1-2	Programming Matrix and Pin Selection Simplified Schematic Diagram	1-6
1-3	Programming Matrix	1-7
1-4	Clock Amplifier Simplified Schematic Diagram	1-10
1-5	VIN LOW Supply Circuit Simplified Schematic Diagram	1-11
1-6	Current Source Circuit Simplified Schematic Diagram	1-13
1-7	Current Sink Circuit Simplified Schematic Diagram	1-14
1-8	Positive Logic NAND Gate Typical Specifications	1-15
1-9	Positive Logic Flip-Flop Typical Specifications	1-20
1-10	Motorola MC1013P J-K Flip-Flop Specifications	1-22
1-11	Power Supply Voltage Adjustments	1-27
1-12	I SINK and I SOURCE Adjustments	1-28

LIST OF TABLES

Table Number	Description	Page
1-1	Salient Characteristics	1-2

BECKMAN MODEL 999

INTEGRATED CIRCUIT (IC) TESTER

1.0 INTRODUCTION

The Beckman Model 999 IC Tester checks all important parameters of integrated circuits: RTL, RCTL, DTL, modified DTL, TTL, LPDTL, CML, and ECL. It tests the input threshold levels, output levels, output current (both high and low levels), short-circuit output currents, input forward current, fan out, power dissipation and current drain from the supply, noise immunity, and the truth tables. It gives the exact value of the parameter to be tested.

Because it does not require complicated programming, it is widely used by laboratories, quality control, manufacturing, and educational facilities. Anyone knowledgeable of IC's can quickly set up and operate the IC Tester. Anyone studying IC's can use the Tester for practical demonstrations of integrated circuit theory. The student can learn and check the characteristics of all digital integrated circuits.

1.1 SPECIFICATIONS

The specifications of the Model 999 IC Tester are listed in Table 1-1.

Table 1-1. Salient Characteristics

Vcc:

+ 5 V ±2%	0-200 ma
+ 12 V ±2%	0-200 ma
0 to 10 V	0-200 ma

Current Source:

50 μa to 100 ma adjustable in 3 ranges.

Current Sink:

50 μa to 100 ma adjustable in 3 ranges.

Clock:

100 KHz (internal)
Manual
DC to 1 MHz (external)
(Voltage swings between Vin High and Vin low)

Vin High:

0 to 10 V adjustable
0 to 50 ma

Vin Low:

0 to 10 V adjustable
0 to 50 ma

Meter:

Any pin of I.C. socket may be monitored. Meter has two voltage ranges:

0 to 10 V ±2%
0 to 2.5 V ±2%

The meter also measures I source and I sink with full scale ranges of 1, 10 and 100 ma.

Test Set Up Switch:

In set up position all power is removed from I.C.

External Monitor:

A scope or digital voltmeter may be used to monitor any pin of I.C.

Types of I.C. Packages Accepted

14 pin dual-in-line	(option C-1)
16 pin dual-in-line	(option C-2)
8 pin TO-5	(option C-3)
10 pin TO-5	(option C-4)
12 pin TO-5	(option C-5)
14 pin TO-5	(option C-6)
14 pin 1/4" x 1/4" flat-pack	(option C-7)
14 pin 1/8" x 1/4" flat-pack	(option C-8)

Input Voltage:

115/230 VAC (switch selected)
50 to 1000 Hz

Input Power:

10 W

Operating Temperature:

0 to 50°C

Size:

16 1/2" W, 7" H and 12 1/4" deep

Weight:

Approximately 10 lbs.

Price:

Basic unit (not including optional socket adapters)

$495.00

Options:

Optional adapters C-1 through C-8 available at $14.50 each.

1.2 PROGRAMMING AND CONTROLS

Checking the various parameters of integrated circuits generally involves applying known levels to the inputs and then observing the outputs. In the Beckman Model 999 IC Tester, different voltage and logic levels are applied to the IC under test in several configurations. The routing of the signals to any pin of the IC under test is accomplished by a programming matrix. Voltage and logic levels are adjusted individually while being monitored by a front-panel meter, or by an externally-connected instrument. The meter, the programming matrix, and the operating controls are illustrated in Figures 1-1 and 1-3. The use of these items is described in the following paragraphs. Efficient use of the IC Tester is enhanced by understanding the operation and limitations of the controls.

1.3 METER PANEL

The upper portion of the control panel (Figure 1-1) is the meter panel. The meter panel includes a 100-microampere meter, a 16-position PIN SELECTOR rotary switch, two RANGE selector switches, and the EXT MONITOR terminal posts.

1.3.1 METER

The meter indicates voltage or current, depending upon the setting of the four-position RANGE selector switch. In the first two positions, the meter indicates 2.5 volts and 10 volts full-scale, respectively. In the I SOURCE position, the meter indicates the amount of current drawn by the IC under test from a constant-current source. The current may be 1, 10, or 100 milliamperes full-scale, depending upon the setting of the three-position RANGE selector switch.

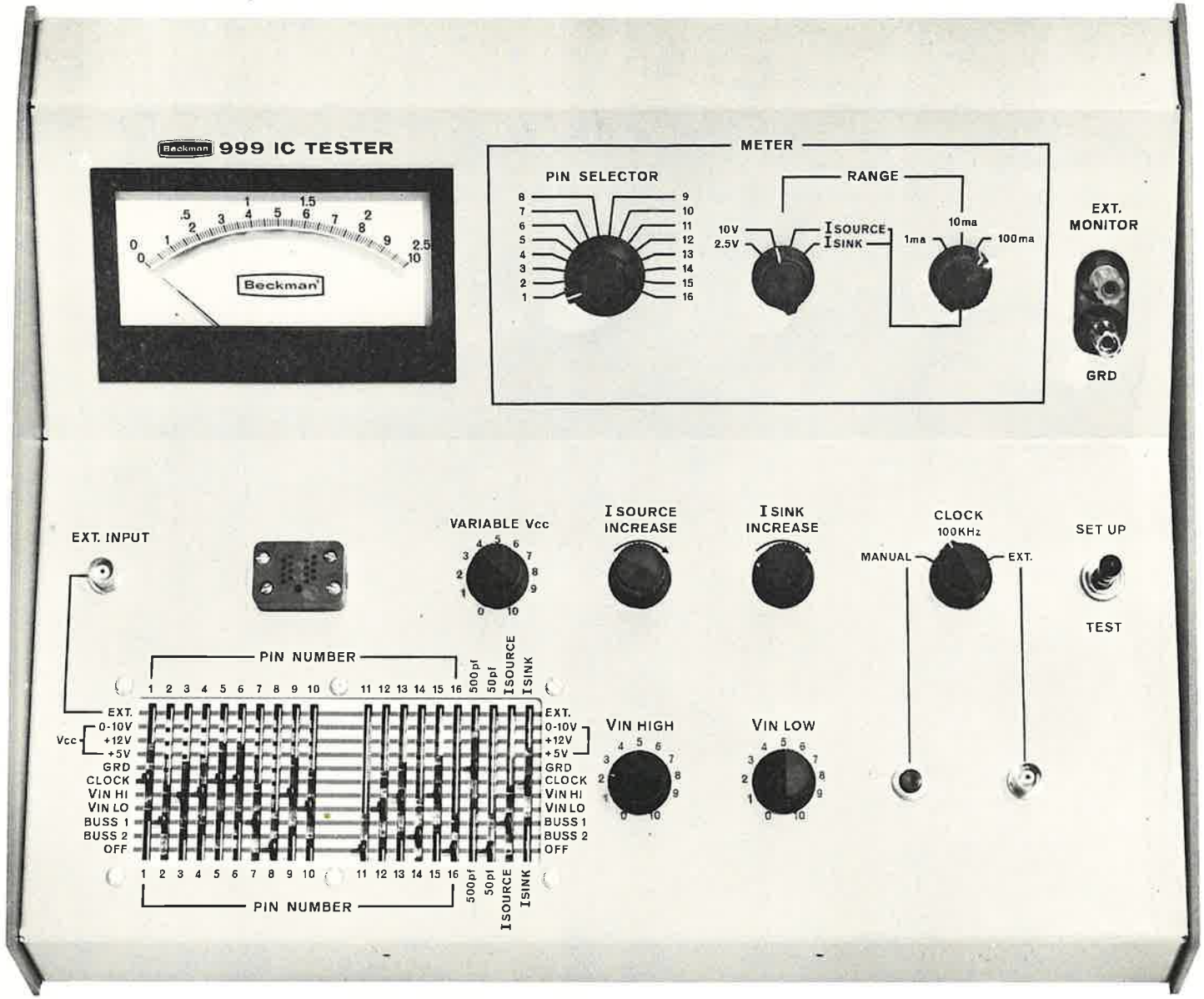


Figure 1-1. Operating Controls

1.3.2 RANGE

In the I SINK position, the meter measures the current flowing out of the IC under test into a current sink. This current may be 1, 10, or 100 milliamperes, depending upon the setting of the three-position RANGE selector switch. The amount of current flowing out of or into the IC under test does not exceed the value selected by the three-position RANGE selector switch.

1.3.3 PIN SELECTOR

Voltage and current measurements can be made at any pin of the IC under test. As shown in Figure 1-2, the PIN SELECTOR rotary switch provides access to each pin of the IC under test. The arm of the switch directs the pin selected directly to the voltmeter positions of the four-position RANGE selector switch. Current measurements are made in a similar manner; the method is described in paragraph 1.5.1.4.

The signal selected by the PIN SELECTOR rotary switch appears on the EXT MONITOR terminal posts. Consequently, every pin of the IC under test can be brought out of the instrument for further analysis by an external digital voltmeter, oscilloscope, etc.

1.4 CONTROL PANEL

The control panel includes a programming matrix, an IC adapter socket, and various controls for setting up the test parameters. The IC under test plugs into an adapter, and the adapter plugs into the IC adapter socket. Adapters are optionally provided with the instrument to accomodate all IC packages currently on the market.

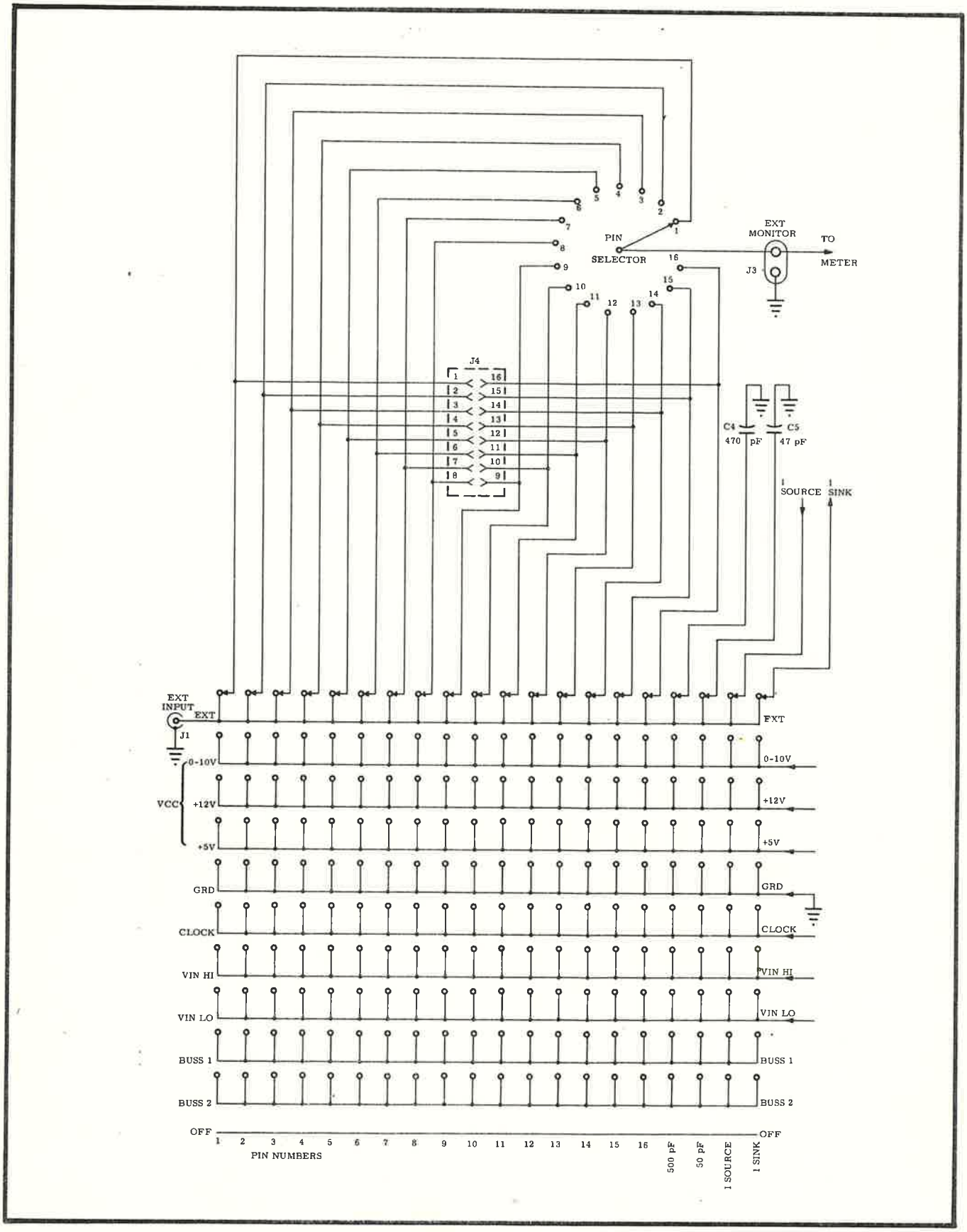


Figure 1-2. Programming Matrix and Pin Selection Simplified Schematic Diagram

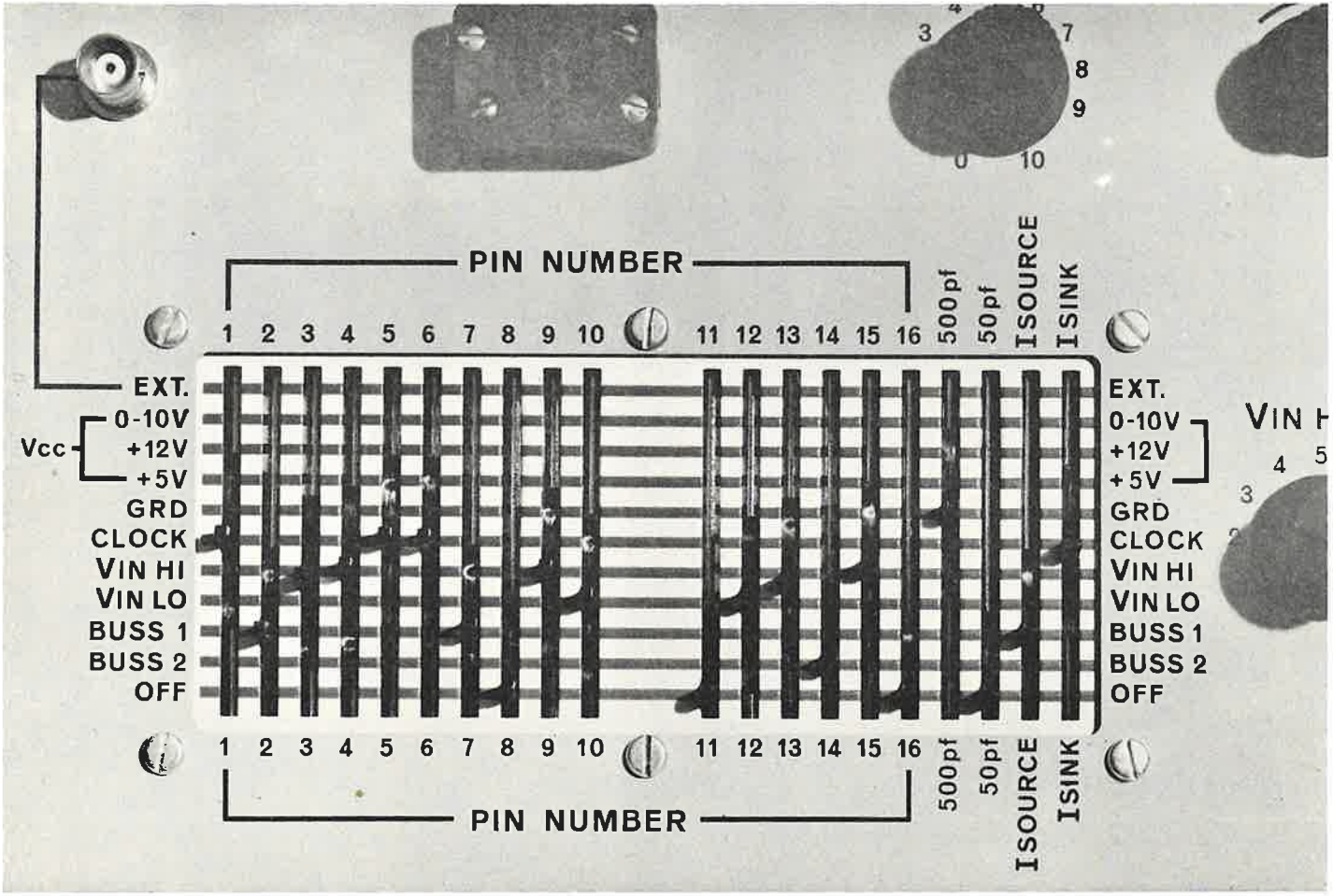


Figure 1-3. Programming Matrix

1.4.1 PROGRAMMING MATRIX

Figure 1-2 is a simplified schematic diagram of the programming matrix. Figure 1-3 shows the physical arrangement of the programming matrix.

The programming matrix, in effect, is made up of 20 separate 11-position slider switches. The positions of the switches are indicated by horizontal lines. At either end of the horizontal lines is indicated the function or signal associated with that position of the switch.

The vertical lines through the programming matrix represent the arms of the switches. Associated with the first 16 switches are the pins of the IC adapter socket. The other four switches are for a 500-pf load, a 50-pf load, a current source, and a current sink; in that order.

Signals are applied to the various pins of the IC under test by sliding the corresponding switches to the signal or function positions. Thus, to apply the clock to pin 10 of the IC under test, simply slide the PIN NUMBER 10 switch to the CLOCK position. The various signals and interconnections that are present at the programming matrix are described in the following paragraphs in the order that they appear on the programming matrix.

1.4.2 EXT.

The EXT. position is a direct line to the EXT. INPUT connector. This position is available for introducing into the instrument a signal that is not supplied by the IC tester. It can also be used to interconnect pins or to connect an external load, which can then be connected to any pin.

1.4.3 VCC 0-10V

The VCC 0-10V position supplies to the programming matrix a variable voltage from 0 to 10 volts DC. The amplitude of this voltage is controlled by the VARIABLE VCC control. No voltage is applied until the SET UP/TEST lever switch is in the TEST position.

1.4.4 VCC +12V

The VCC +12V position supplies a constant DC supply to the programming matrix. The +12V supply is current limited to 200 milliamperes. This power supply can be adjusted by an internal control (R14). The +12V is not applied until the SET UP/TEST lever switch is in the TEST position.

1.4.5 VCC +5V

The VCC +5V position is another DC supply. The +5V supply is also current limited to 200 milliamperes. The voltage can be adjusted by an internal control (R7). The +5V is not applied until the SET UP/TEST lever switch is in the TEST position.

1.4.6 GRD

The GRD position is the reference point for all voltages of the IC tester.

1.4.7 CLOCK

The clocking signal selected by the CLOCK selector switch appears at the CLOCK position. If the CLOCK selector switch is set to MANUAL, the clock pulses are generated one-at-a-time, each time the pushbutton switch under the MANUAL position is pressed momentarily. In the 100KHz position, the clocking signal is supplied by an internal oscillator. The rise time of

this clock is approximately 30 nanoseconds. In the EXT position, an external clock can be introduced into the IC Tester. The maximum external clock frequency is 1 MHz.

Figure 1-4 is a simplified schematic diagram of the clock amplifier. The signal input to the amplifier comes from the arm of the CLOCK selector switch. The output of the amplifier is obtained from the collectors of transistors Q4 and Q6, and it goes directly to the CLOCK position of the programming matrix. The clock swings between the VIN HI and VIN LO levels, which are adjusted by the VIN HIGH and VIN LOW controls, respectively. The maximum level for VIN HI is approximately 10 volts; the minimum level for VIN LO is approximately 0.0 volts.

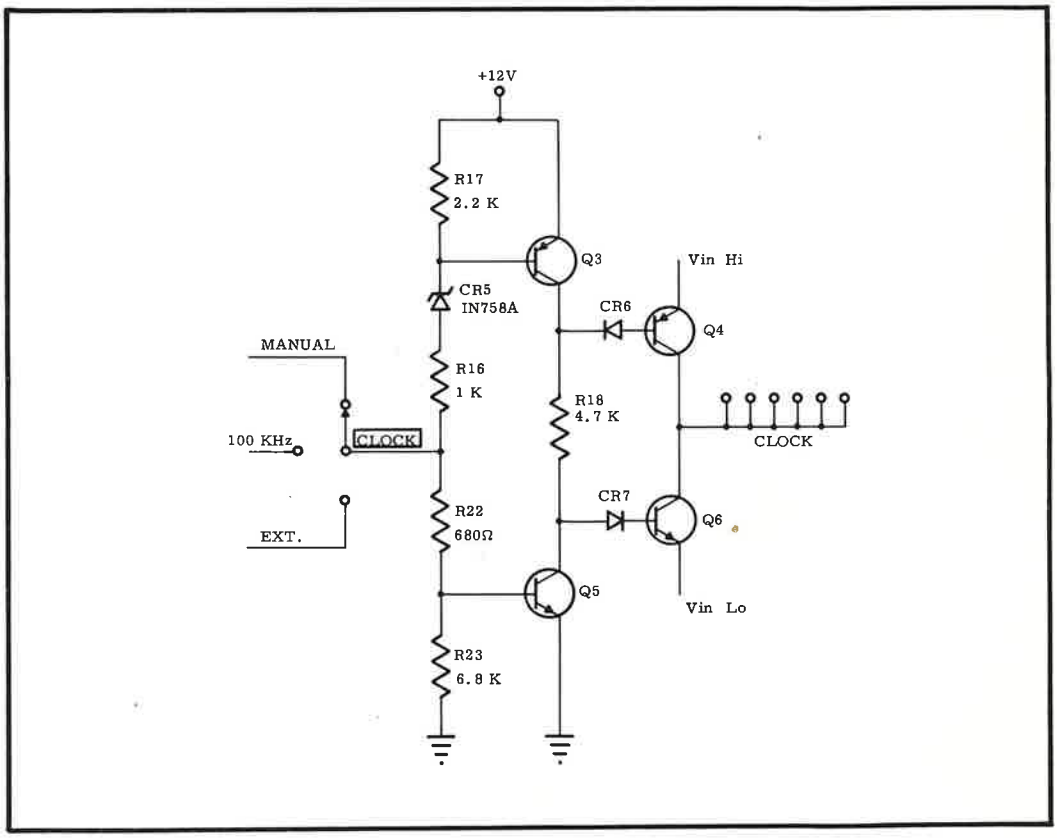


Figure 1-4. Clock Amplifier Simplified Schematic Diagram

1.4.8 VIN HI AND VIN LO

The VIN HI and VIN LO positions supply variable voltages that are controlled by the VIN HIGH and VIN LOW controls, respectively. The circuits producing these levels are identical, and are as illustrated by Figure 1-5, a simplified schematic diagram of the VIN LO supply. The output levels are adjustable from approximately 0.0 to 10.0 volts.

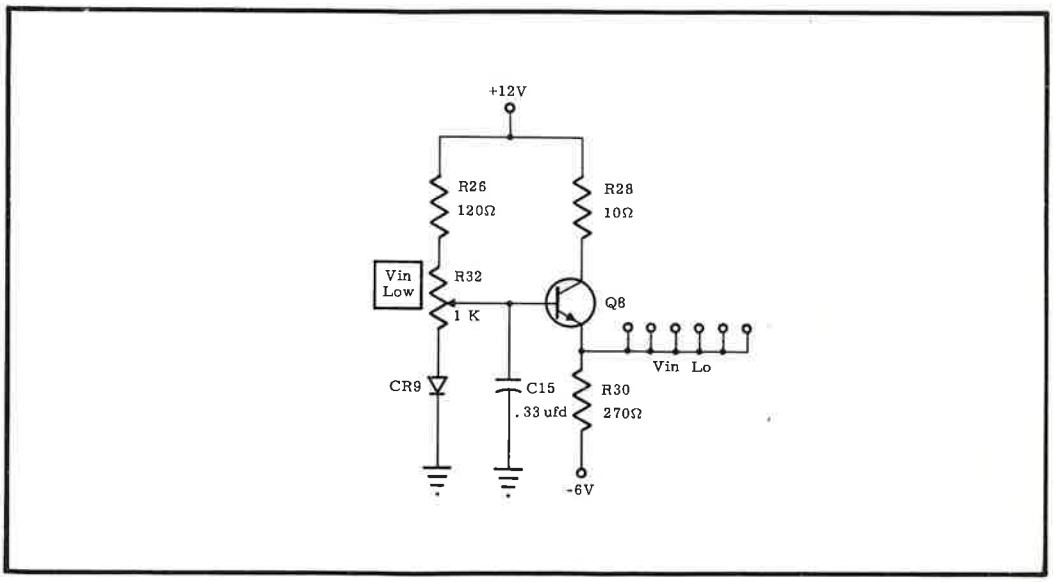


Figure 1-5. VIN LOW Supply Circuit Simplified Schematic Diagram

1.4.9 BUSS 1 AND BUSS 2

The BUSS 1 and BUSS 2 positions serve as interconnecting lines between pins of the IC under test, or they can be used to provide a 500 pf load, a 50 pf load, a current source, or a current sink. When used as interconnecting lines, the switches corresponding to the pin numbers to be interconnected are positioned on the same BUSS line. For the other applications, the switch that provides the function is first set to either BUSS line. The PIN NUMBER switches can then be moved to that BUSS line as required.

For example, assume that a current source must be directed to pin number 11, and pin number 13 must be observed when it is driving a 500-pf load. The set up is made as follows:

a. The 500 pf switch is set to BUSS 1.

b. The I SOURCE switch is set to BUSS 2.

c. The PIN NUMBER 11 switch is set to the BUSS 2 position.

d. The PIN NUMBER 13 switch is set to the BUSS 1 position.

With the switches in these positions, it is then possible to monitor voltage, waveforms, or current; depending on specific measurement requirements.

1.4.10 500 pf AND 50 pf LOADS

The vertical positions designated 500 pf and 50 pf constitute capacitive loads that are generally applied to the EXT, BUSS 1, or BUSS 2 lines as described in the preceding paragraph. The loads are furnished by capacitors C4 and C5, respectively (Figure 1-2).

1.4.11 I SOURCE

A constant-current source is provided on the IC Tester by the I SOURCE switch. This switch is generally positioned on the EXT, BUSS 1, or BUSS 2 lines. The line at which it is placed then becomes the current source for any of the pins of the IC under test.

Figure 1-6 is a simplified schematic diagram of the current source circuit. The amount of current supplied by the circuit is adjusted by the I SOURCE control. The +12-volt supply to the circuit is

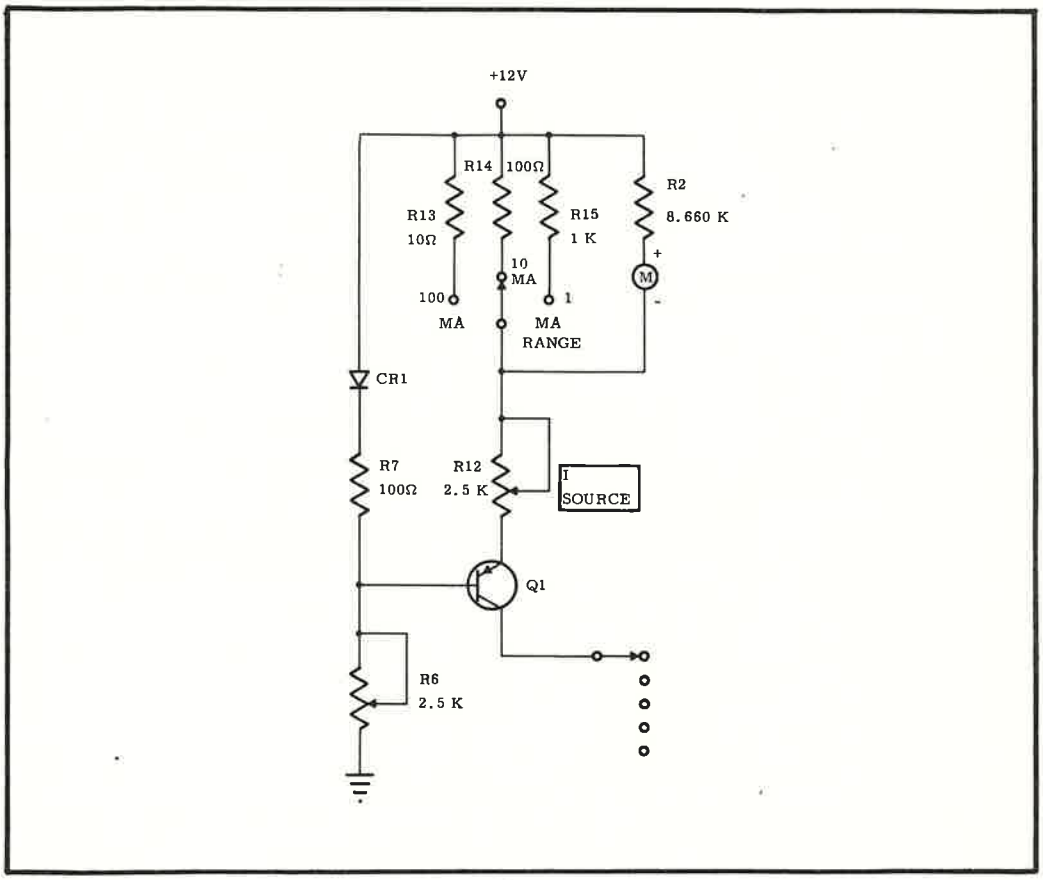


Figure 1-6. Current Source Circuit Simplified Schematic Diagram

applied only when the SET UP/TEST lever switch is in the TEST position.

1.4.12 I SINK

A current sink is provided on the IC Tester by the I SINK switch. This switch is generally positioned on the EXT, BUSS 1, or BUSS 2 lines. The line at which it is placed then becomes the current sink for any of the pins of the IC under test.

Figure 1-7 is a simplified schematic diagram of the current sink circuit. The amount of current drawn by the circuit is adjusted by the I SINK control. The -6-volt supply is applied to the circuit only when the SETUP/TEST lever switch is in the TEST position.

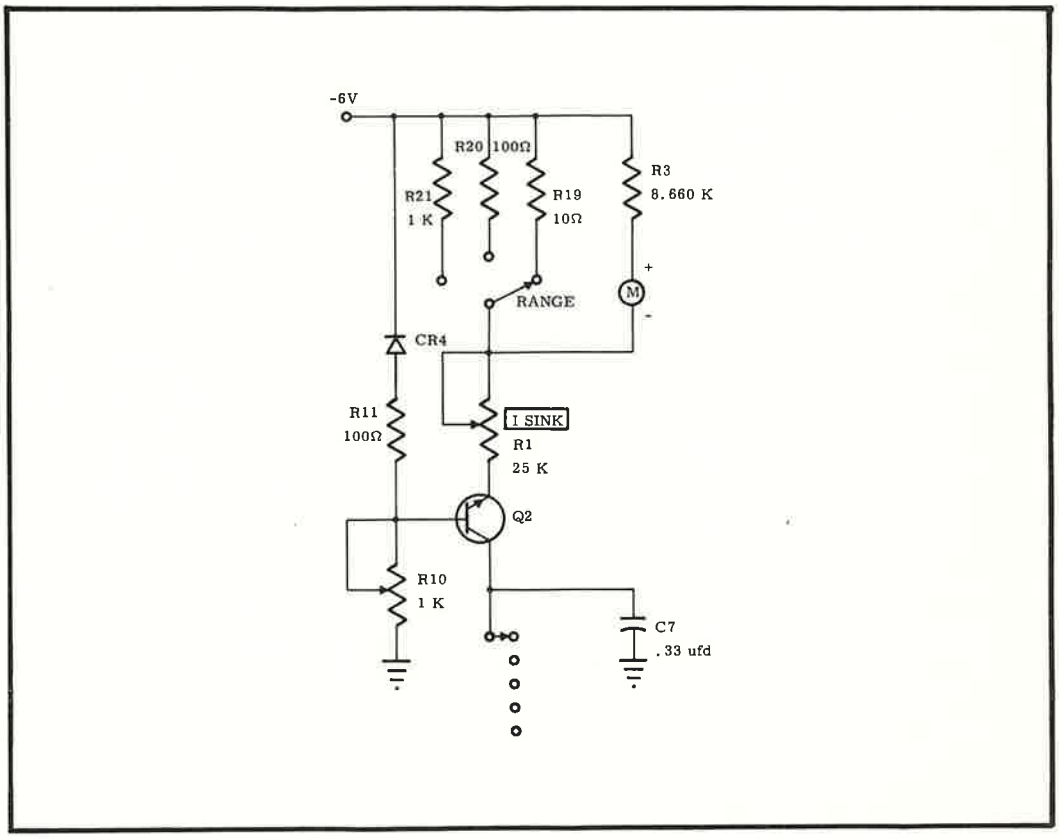
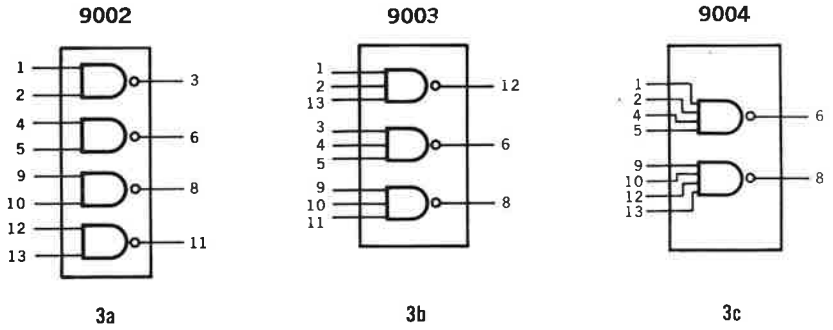


Figure 1-7. Current Sink Circuit Simplified Schematic Diagram

1.5 INTEGRATED CIRCUITS MEASUREMENTS

The use of the Model 999 IC Tester is illustrated by examples. In the first example a Fairchild 9002 NAND gate (positive logic) is checked in accordance with the conditions specified in Figure 1-8. The pin connections and the electrical characteristics of this gate element are given in Figure 1-8.

PIN CONFIGURATION



V_{CC} = PIN 14 GND = PIN 7

ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LIMITS 25°C MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4	2.7		Volts	V_{CC} = 4.5 V, I_{OH} = 1.0 mA V_{IL} = value indicated below on this table.
V_{OL}	Output Low Voltage		0.2	0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 17.6 mA V_{CC} = 4.5 V, I_{OL} = 14.5 mA
V_{IH}	Input High Voltage	1.7			Volts	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage			0.9	Volts	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		−1.10	−1.76	mA	V_{CC} = 5.5 V; V_F = 0.4 V, V_R = 4.5 V on other inputs
I_F	Input Load Current		−0.97	−1.45	mA	V_{CC} = 4.5 V; V_F = 0.4 V, V_R = 4.5 V on other inputs
I_R	Input Leakage Current		20	60	μA	V_{CC} = 5.5 V, V_R = 4.5 V, Gnd. on other inputs
t_{pd+}	Turn Off Delay	4.0		12	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{pd-}	Turn On Delay	3.0		10	ns	V_{CC} = 5.0 V, C_L = 15 pF

Figure 1-8. Positive Logic NAND Gate Typical Specifications

1.5.1 TYPICAL NAND GATE TESTING

1.5.1.1 Output Low Voltage

1. Set all programming matrix switches to the OFF position.
2. Set the appropriate PIN NUMBER switches (1, 2, 4, 5, 9, 10, 12, and 13) to the VIN HI position.

3. Set the PIN NUMBER 7 switch to the GRD position.
4. Set the PIN NUMBER 14 switch to the 0-10V position.
5. Set the four-position RANGE selector switch to the 10V position.
6. Set the PIN SELECTOR rotary switch to 14.
7. Set the VARIABLE VCC control fully counter-clockwise.
8. Hold the SET UP/TEST lever switch in the TEST position and adjust the VARIABLE VCC control to obtain 4.5 volts on the meter.
9. Set the PIN SELECTOR rotary switch to 13.
10. Hold the SET UP/TEST lever switch in the TEST position and adjust the VIN HIGH control to obtain 1.7 volts on the meter.
11. Set the PIN NUMBER 13 switch to VIN LO.
12. Hold the SET UP/TEST lever switch in the TEST position and adjust the VIN LOW control to obtain 0.9 volts on the meter.
13. Return the PIN NUMBER 13 switch to the VIN HI position.
14. Plug the IC to be tested into the appropriate adapter and plug the adapter into the adapter socket, being careful to observe correct pin connections.
15. Measure the output voltages at pins 3, 6, 8, and 11 by setting the PIN SELECTOR switch to those positions. Measurements are made with the SET UP/TEST lever switch in the TEST position, and the four-position RANGE switch in the 2.5V position. The output low voltage should not exceed 0.4 volts.

1.5.1.2 Output High Voltage

1. Set PIN NUMBER switches 1, 4, 9, and 12 to the VIN LO position.
2. Measure the output voltages at pins 3, 6, 8, and 11. The minimum level is 2.4 volts.
3. Return PIN NUMBER switches 1, 4, 9, and 12 to the VIN HI position; set PIN NUMBER switches 2, 5, 10, and 13 to the VIN LO position.
4. Measure the output voltages at pins 3, 6, 8, and 11. The output levels should be the same as measured in step 2 above.

1.5.1.3 Input High Voltage (Threshold Level)

1. Set IC Tester logic inputs as required for checking output low voltage; check outputs and ensure that circuits operate.
2. Measure output level at pin 3; slowly rotate VIN HIGH counter-clockwise to the point where the output goes high.
3. Measure the voltage level at pin 1; it should not exceed 1.7 volts.
4. Repeat test for the other NAND gates.

1.5.1.4 Supply Current

1. Set the IC Tester logic inputs as required for checking output low voltage.
2. Set the PIN NUMBER 14 and the I SOURCE switches to BUSS 1.
3. Rotate the I SOURCE control fully counter-clockwise; set the three-position RANGE selector switch to 100 MA.

4. Monitor the voltage at pin 14; adjust the I SOURCE control until the level is 4.5 volts.

5. Switch the four-position RANGE selector switch to the I SOURCE position to determine load current. If desired, the switching load current can also be determined. Proceed as follows:

   a. Set all input switches to the CLOCK position.

   b. Set the CLOCK selector switch to the 100KHz position.

   c. When the IC is tested, the logic input levels switch between VIN LO and VIN HI. The current drawn by the IC is indicated on the meter. If desired, the output of any NAND gate can be observed on an oscilloscope by connecting it to the EXT MONITOR terminal posts and selecting the outputs with the PIN SELECTOR rotary switch.

1.5.1.5 Input Current

1. Set PIN NUMBER 14 switch to the VCC 0-10V position; adjust VCC to 5.5 volts.
2. Set VIN HI level to 1.7 volts as in paragraph 1.5.1.1.
3. Set PIN NUMBER 2 switch to VIN HI.
4. Set the three-position RANGE selector switch to 10 MA. Check that no switches are on the BUSS 1 line; then set the PIN NUMBER 1 and the I SINK switches to BUSS 1.
5. Rotate I SINK control fully counter-clockwise.
6. Monitor the voltage on pin 1 and rotate the I SINK control to obtain 0.4 volts.

7. Set the four-position RANGE selector switch to I SINK and measure the input load current. It should not exceed -1.76 milliamperes.

8. Repeat test for the other NAND gates.

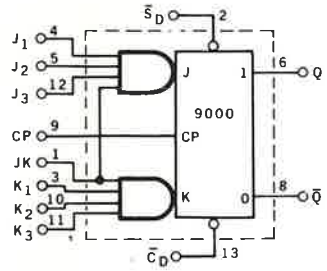
1.5.2 TYPICAL FLIP-FLOP TESTING

In the second example a Fairchild 9000 J-K flip-flop is checked as specified in Figure 1-9. The pin connections, the electrical characteristics, and the truth tables of the flip-flop are given in the figure.

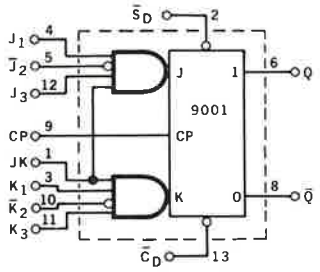
1.5.2.1 J-K Mode Operation (9000, Figure 1-9)

1. Set VCC level to 4.5 volts as described in paragraph 1.5.1.1.
2. Set VIN HI to 1.7 volts as described in paragraph 1.5.1.1.
3. Set VIN LO to 0.9 volts as described in paragraph 1.5.1.1.
4. Set PIN NUMBER 14 switch to the 0 - 10 volt position.
5. Set PIN NUMBER 7 switch to the GRD position.
6. Set all other PIN NUMBER switches, except 6, 8, and 9, to the VIN HI position.
7. Set PIN NUMBER 9 switch to the CLOCK position.
8. Set the CLOCK selector switch to the MANUAL position.

J-K FLIP-FLOPS — 9000, 9001



VCC = PIN 14
GND = PIN 7



V_{CC} = PIN 14
GND = PIN 7

LOADING RULES

FLIP-FLOP INPUTS	LOADING*
CP, J_1, J_2, J_3, K_1, K_2, K_3, $\overline{J}_2$, $\overline{K}_2$,	1
JK	2
$\overline{S}_D$, $\overline{C}_D$	2.7

OUTPUTS	FAN-OUT
Q, $\overline{Q}$	10

*1 load = 1 TTμL Gate Input Load

ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = 1.0 mA, V_{IL} on asynchronous input	
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 14.5 mA V_{CC} = 5.5 V, I_{OL} = 17.7 mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs	
I_R 2 I_R I_{RS}	Input Leakage Current J, K, J, K & Clock Inputs J-K Input Asynchronous Inputs				20 40 55	60 120 162		100 200 270	μA	V_{CC} = 5.5 V, V_R = 4.5 V, Gnd. on other inputs	
I_F 2 I_F I_{FSI}	Input Load Current J, K, J, K & Clock Inputs J-K Input Asynchronous Inputs		−1.76 −3.52 −4.75		−1.1 −2.2 −3.0	−1.76 −3.52 −4.75		−1.76 −3.52 −4.75	mA	V_{CC} = 5.5 V V_{CC} = 5.5 V V_{CC} = 5.5 V	V_F = 0.4 V V_R = 4.5 V on other inputs
I_F 2 I_F I_{FSI}	Input Load Current J, K, J, K & Clock Inputs J-K Input Asynchronous Inputs		−1.45 −2.9 −3.92		−0.91 −1.82 −2.48	−1.45 −2.9 −3.92		−1.45 −2.9 −3.92	mA	V_{CC} = 4.5 V V_{CC} = 4.5 V V_{CC} = 4.5 V	
t_{pd+}				—	12	20			ns	9000 or 9001	V_{CC} = 5.0 V C_L = 15 pF See test circuits and curves.
t_{pd-}				—	18	30			ns	9000 or 9001	
$t_{release}$					5	1			ns	9001 only	
t_{set-up}				10	6				ns	9001 only	
	Negative Clock pulse width			15	10				ns	9001 only Toggle condition	

TRUTH TABLES

SYNCHRONOUS ENTRY
J-K MODE OPERATION

JK	J_1 • (5) J_2 • J_3	K_1 • (5) K_2 • K_3	Q	$\overline{Q}$
	INPUTS @ t_n		OUTPUTS @ t_{n+1}	
1	4 5 12	3 10 11	6	8
L	X	X	No Change (4)	
H	L	L	No Change (4)	
H	L	H	L	H
H	H	L	H	L
H	H	H	Toggles	

ASYNCHRONOUS ENTRY
Independent of Clock and Synchronous Input

S_D	C_D	Q	$\overline{Q}$
INPUTS		OUTPUTS	
2	13	6	8
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

NOTES:
(1.) H = Most positive logic level.
(2.) L = Most negative voltage level.
(3.) X = Could be high or low.
(4.) For no change of outputs, the J and K inputs or the common JK input must remain low from the time the clock goes low to the time the clock goes high again.
(5.) The 9001 has inverted J_2 (Pin 5) and K_2 (Pin 10) inputs. When not in use, they must be grounded.

Figure 1-9. Positive Logic Flip-Flop Typical Specifications

9. Plug the IC to be tested into the appropriate adapter and plug the adapter into the adapter socket, being careful to observe correct pin connections.

10. Measure the output voltages at pins 6 and 8. The output that is "true" at this particular time should be at least 2.4 volts; the opposite output should not be greater than 0.4 volts. Note these values.

11. Set the CLOCK selector switch to 100KHz.

12. Measure the output voltages again; they should be at some value between the levels recorded in step 10 above.

13. The output waveforms may be observed by connecting an oscilloscope to the EXT. MONITOR terminal posts.

1.5.2.2 Logic Gate Operation

1. Ascertain that flip-flop toggles by performing the instructions of paragraph 1.5.2.1.

2. Set the CLOCK selector switch to MANUAL.

3. Connect the flip-flop inputs in accordance with the first logic conditions defined by the truth table.

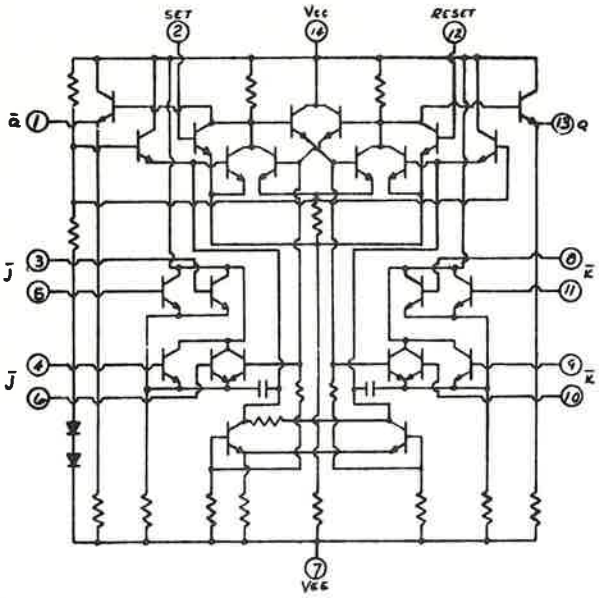
4. Generate a clock pulse manually and observe that outputs are in agreement with truth table.

5. Repeat steps 3 and 4 above for each logic condition as defined by the truth table.

1.5.3 EXTENSIVE FLIP-FLOP TESTING

In the third example, a Motorola MC1013P J-K Flip-Flop is checked as specified in Figure 1-10. The pin connections, the electrical characteristics, and the truth tables of the flip-flop

CIRCUIT SCHEMATIC

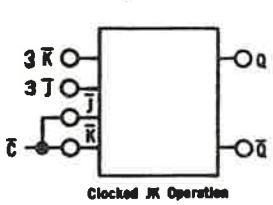


MECL* Series

Integrated Circuits

70MHz AC COUPLED J-K FLIP-FLOP

LOGIC DIAGRAM



J	K	C	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q^n}$
0	1	1	1
1	0	1	0
1	1	1	Q^n

The J and K inputs refer to logic levels while the C input refers to dynamic logic swings. The J and K inputs should be changed to a logical "1" only while the C input is in a logic "1" state.

PRELIMINARY SPECIFICATIONS

MC1013P

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{EE}	-10	Vdc
Output Source Current	I_o	20	mAdc
Operating Temperature	T_A	0 to +75	°C
Storage Temperature	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS

@V_{EE} = -5.2Vdc ±10%, V_{CC} = 0Vdc, All unused inputs connected to -5.2Vdc.

		0°C		25°C		75°C		
CHARACTERISTIC	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply Drain Current, I_E					29			mAdc
Input Current, I_{IN}	V_{IN} = -0.680Vdc				100			µAdc
"Q" Logical "1" Output Voltage, V_{OH}	V_{IN}(set)[1]	-0.850	-0.695	-0.800	-0.680	-0.725	-0.570	Vdc
"Q" Logical "0" Output Voltage, V_{OL}	V_{IN}(reset)[2]	-1.880	-1.510	-1.800	-1.465	-1.730	-1.395	Vdc
"$\overline{Q}$" Logical "1" Output Voltage, V_{OH}	V_{IN}(reset)[2]	-0.850	-0.695	-0.800	-0.680	-0.725	-0.570	Vdc
"$\overline{Q}$" Logical "0" Output Voltage, V_{OL}	V_{IN}(set)[1]	-1.880	-1.510	-1.800	-1.465	-1.730	-1.395	Vdc
"Q" and "$\overline{Q}$" Logical "1" Output Voltage, V_{OH}(f1)	I_L = -2.5mAdc	-0.935	-0.695	-0.855	-0.680	-0.790	-0.570	Vdc
Toggle Frequency	50% Duty Cycle			70				MHz

1. V_{IN}(set)= V_{OH} then V_{OL}(max) 2. V_{IN}(reset)= V_{OH} then V_{OL}(max)

Figure 1-10. Motorola MC1013P J-K Flip-Flop Specifications

are given in the figure, with the exception that Vee is 0V DC and Vcc is +5.2V. DC. Readings should be transposed accordingly.

1.5.3.1 J-K Mode Operation

1. Set VCC level to 5.2 volts as described in paragraph 1.5.1.1.
2. Set VIN HI to 4.40 volts as described in paragraph 1.5.1.1.
3. Set VIN LO to 3.74 volts as described in paragraph 1.5.1.1.
4. Set PIN NUMBER 14 switch to the 0 - 10 volt position.
5. Set PIN NUMBER 7 switch to the GRD position.
6. Set all other PIN NUMBER switches, except 1, 3, 8 and 13, to the VIN LO position.
7. Set PIN NUMBER 3 and 8 switches to the CLOCK position.
8. Set the CLOCK selector switch to the MANUAL position.
9. Plug the IC to be tested into the appropriate adapter and plug the adapter into the adapter socket, being careful to observe correct pin connections.
10. Measure the output voltages at pins 1 and 13. The output that is "true" at this particular time should be at least 4.40 volts; the complement output should not be greater than 3.74 volts. Note these values.
11. Set the CLOCK selector switch to 100 kHz.
12. Measure the output voltages again; they should be at some value between the levels recorded in step 10 above.
13. The output waveforms may be observed by connecting an oscilloscope to the EXT. MONITOR terminal posts.

1.5.3.2 Truth Logic

1. Set the I.C. TESTER logic inputs as specified in paragraph 1.5.3.1.
2. Slide PIN NUMBERS 3 and 8 switches to VIN LO.
3. Monitor Pins 1 and 13. One of the pins should be approximately 3.7 volts; the other pin should be approximately 4.4 volts.
4. Slide PIN NUMBERS 3 and 8 switches to CLOCK.
5. Monitor Pins 1 and 13. Set the CLOCK switch to MANUAL. Depress the MANUAL Pushbutton switch. The output low voltage should be approximately 3.7 volts and the output high voltage should be approximately 4.4 volts.
6. Slide PIN NUMBER 9 switch to VIN HI.
7. Monitor Pin 1. Depress the MANUAL Pushbutton switch. The output voltage should go to approximately 3.7 volts and remain at this level.
8. Monitor Pin 13. Depress the MANUAL Pushbutton switch. The output voltage should go to approximately 4.4 volts and remain at this level.
9. Slide PIN NUMBER 9 switch to VIN LO and PIN NUMBER 4 switch to VIN HI.
10. Monitor Pin 1. Depress the MANUAL Pushbutton switch. The output voltage should go to approximately 4.4 volts and remain at this level.
11. Monitor Pin 13. Depress the MANUAL Pushbutton switch. The output voltage should go to approximately 3.7 volts and remain at this level.
12. Slide PIN NUMBER 9 switch to VIN HI.

13. Monitor Pins 1 and 13. The output voltage should be approximately 3.7 volts or 4.4 volts according to the state of the Flip-Flop. Depressing the Pushbutton switch should not change the state of the Flip-Flop.

1.5.3.3 Supply Current

1. Set the IC Tester logic inputs as required for typical Flip-Flop testing.
2. Set the PIN NUMBER 14 and the I SOURCE switches to BUSS 1.
3. Rotate the I SOURCE control fully counter-clockwise; set the three-position RANGE selector switch to 100 MA.
4. Monitor the voltage at Pin 14; adjust the I SOURCE control until the level is 5.2 volts.
5. Switch the four-position RANGE selector switch to the I SOURCE position to determine load current. If desired, the switching load current can also be determined. Proceed as follows:
   a. Set all input switches to the CLOCK position.
   b. Set the CLOCK selector switch to the 100 kHz position.
   c. When the IC is tested, the logic input levels switch between VIN LO and VIN HI. The current drawn by the IC is indicated on the meter. If desired, the output of the Flip-Flop can be observed on an oscilloscope by connecting it to the EXT. MONITOR terminal posts and selecting the outputs with the PIN SELECTOR rotary switch.

1.5.3.4 Input Current

1. Set PIN NUMBER 14 switch to the VCC 0-10 V position; adjust VCC to 5.2 volts.
2. Set VIN HI level to 4.4 volts as in paragraph 1.5.1.1.
3. Set the three-position RANGE selector switch to 1 MA. Check that no switches are on the BUSS 1 line; then set the PIN NUMBER 4 and the I SOURCE switches to BUSS 1.
4. Rotate the I SOURCE control fully counter-clockwise.
5. Monitor the voltage on Pin 4 and rotate the I SOURCE control to obtain 4.5 volts.
6. Set the four-position RANGE selector switch to I SOURCE and measure the input load current. It should not exceed 0.1 milliamperes.
7. Repeat this test for the other INPUTS.

1.6 MAINTENANCE

Periodic maintenance of the Model 999 IC Tester is normally not required. The overall stability and reliability of the instrument is such that if it is used properly it will provide years of uninterrupted service. The power supply voltages, the current source circuit, and the current sink circuit may require readjustment after prolonged usage, due to component aging. Procedures for making these adjustments are provided in the following paragraphs. Test points and associated controls are shown in Figures 1-11 and 1-12. All voltages are referenced to ground.

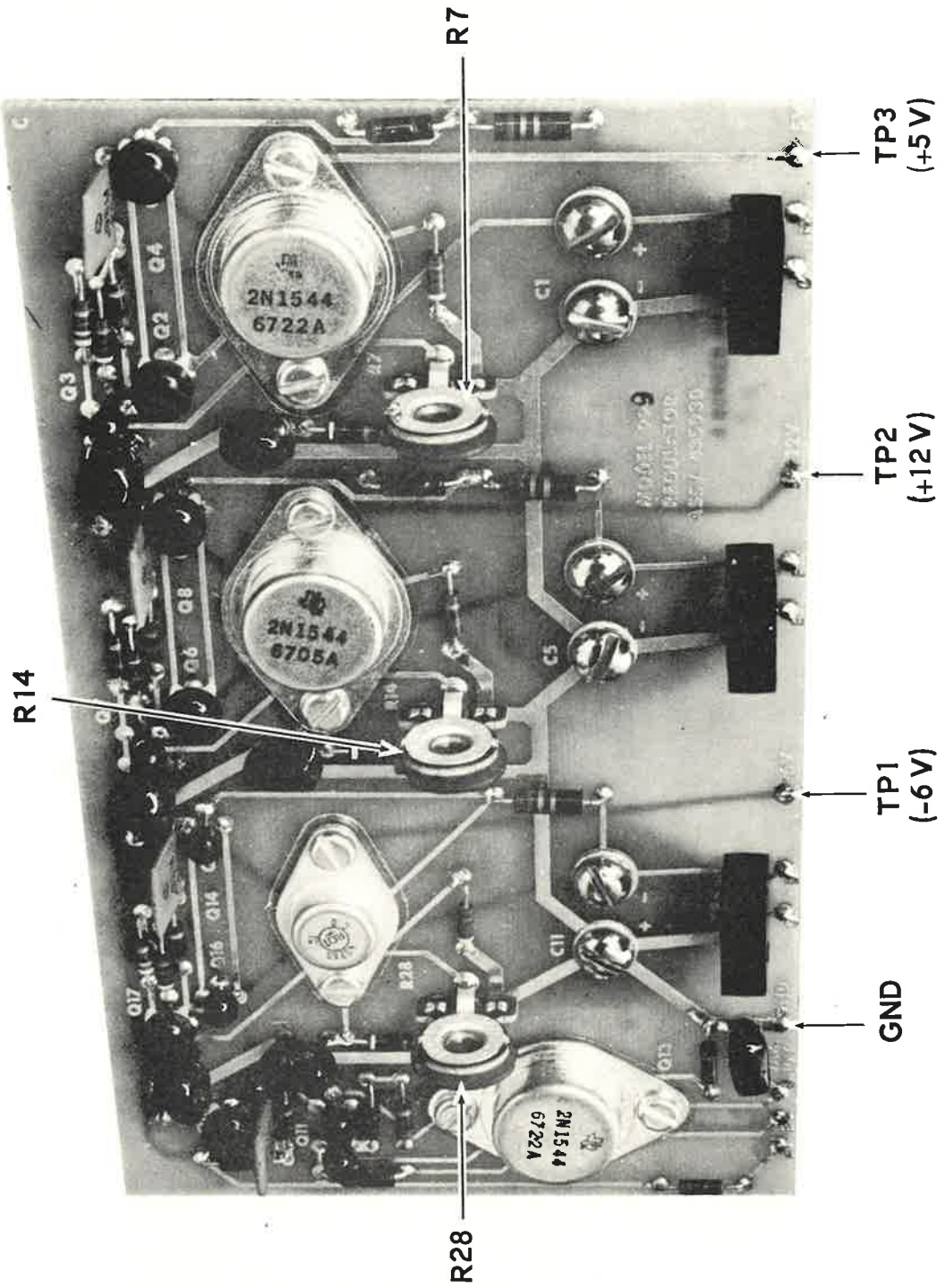


Figure 1-11. Power Supply Voltage Adjustments

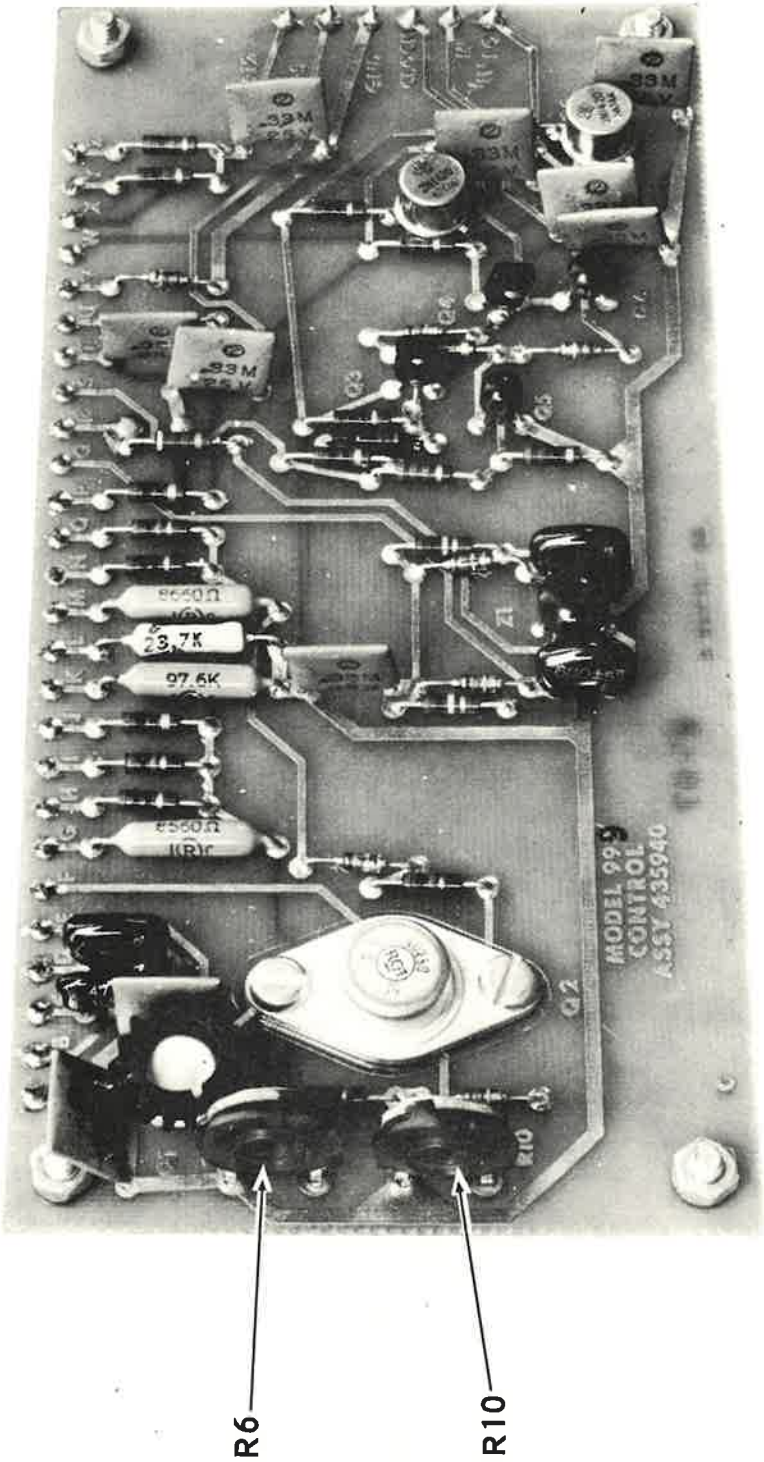


Figure 1-12. I SINK and I SOURCE Adjustments

1.6.1 POWER SUPPLY ADJUSTMENTS

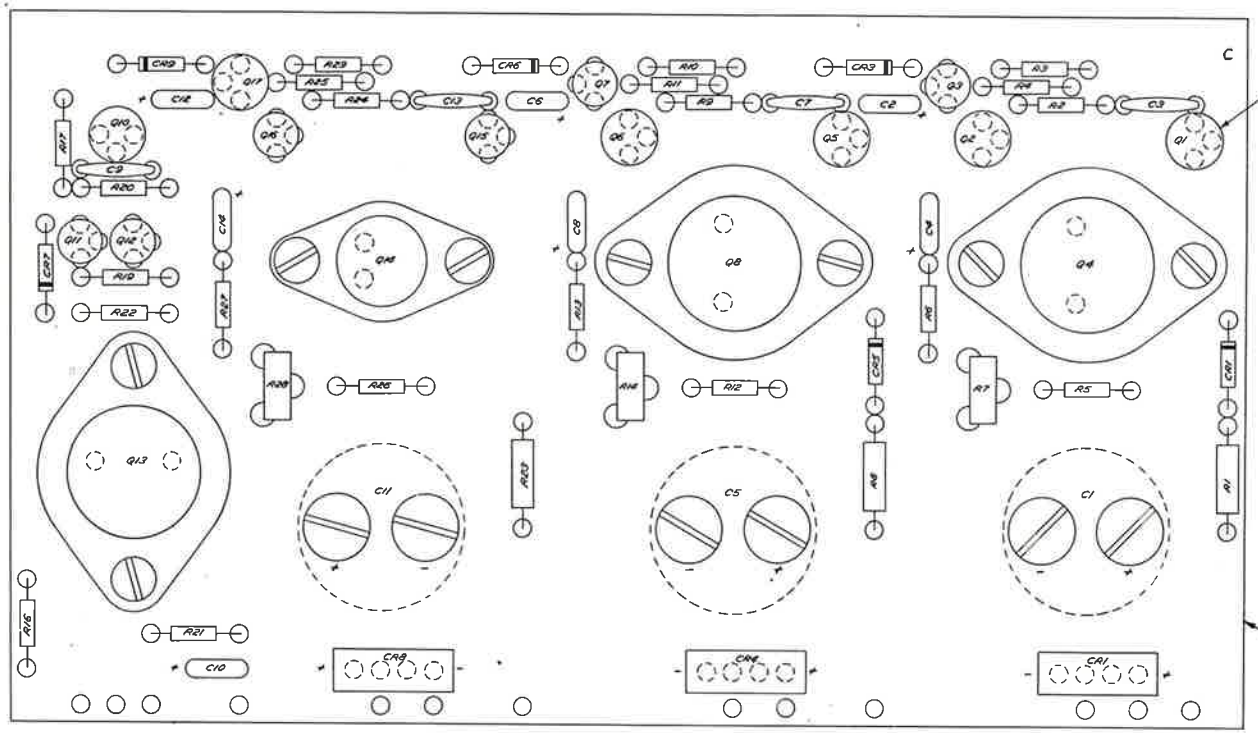
1. Monitor the voltage at TP3 (+5V).
2. Adjust potentiometer R7 to obtain +5 (±1%) volts.
3. Monitor the voltage at TP2 (+12V).
4. Adjust potentiometer R14 to obtain +12 (±1%) volts.
5. Monitor the voltage at TP1 (-6V).
6. Adjust potentiometer R28 to obtain -6 (±1%) volts.

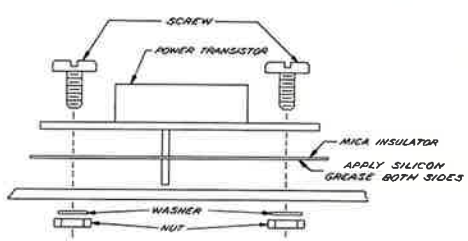
1.6.2 CURRENT SOURCE ADJUSTMENTS

1. Set all PIN NUMBER switches to the OFF position.
2. Ground the center conductor of the EXT. INPUT connector.
3. Set the I SOURCE switch to the EXT. position.
4. Set the RANGE switches to I SOURCE and 100 MA.
5. Set the I SOURCE control fully clockwise.
6. Hold the SET UP/TEST lever switch in the TEST position and adjust potentiometer R6 for full-scale indication on the IC Tester meter.

1.6.3 CURRENT SINK ADJUSTMENT

1. Set all PIN NUMBER switches to the OFF position.
2. Ground the center conductor of the EXT. INPUT connector.
3. Set the I SINK switch to the EXT. position.
4. Set the RANGE switches to I SINK and 100 MA.
5. Set the I SINK control fully clockwise.
6. Hold the SET UP/TEST lever switch in the TEST position and adjust potentiometer R10 for full-scale indication on the IC Tester meter.





NOTE:

C1, C5, C11, Q9, Q8, Q13, Q14, R7, R14, & R18 TO BE INSTALLED & SOLDERED. AFTER WAVE SOLDERING. CLIP TRANSISTOR LEADS AFTER SOLDERING.

D 955-435930

3	0000-435931	SCHEMATIC, POWER SUPPLY	REF.
2	C693-435940	SPECIFICATION DWG, REGULATOR	REF.
1	A037-435929	PARTS LIST, REGULATOR BD.	1
ITEM	PART NO	DESCRIPTION	QTY

BOARD ASSEMBLY, REGULATOR

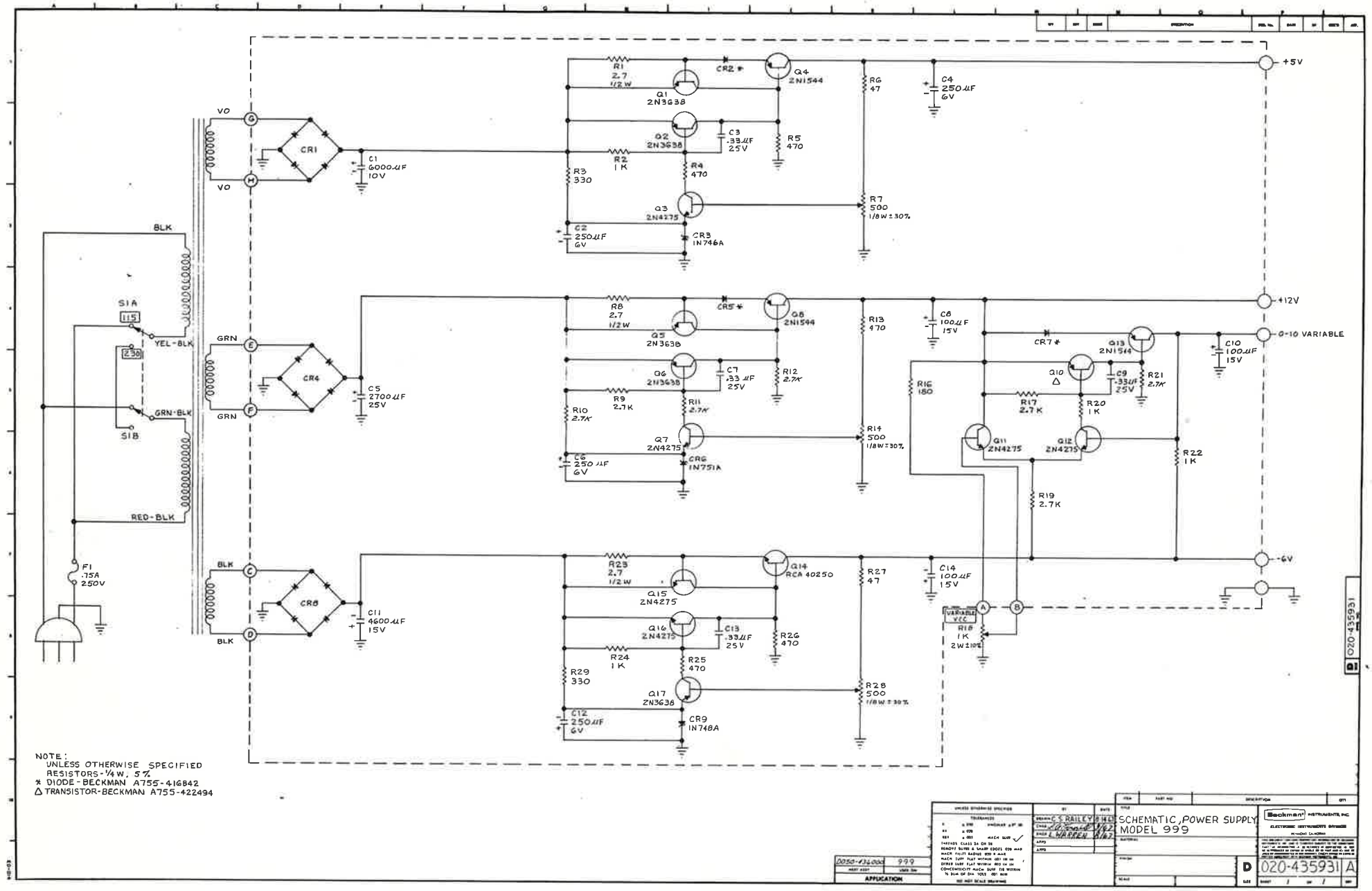
Beckman INSTRUMENTS, INC. ELECTRONIC INSTRUMENTS DIVISION

D 955-435930 A

SCALE 3:1

A855-435907 999

APPLICATION

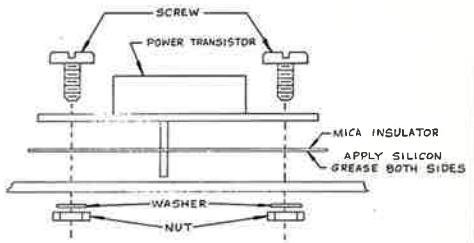


NOTE:
UNLESS OTHERWISE SPECIFIED
RESISTORS - ¼ W, 5%
* DIODE - BECKMAN A755-416842
Δ TRANSISTOR-BECKMAN A755-422494

D 020-435931

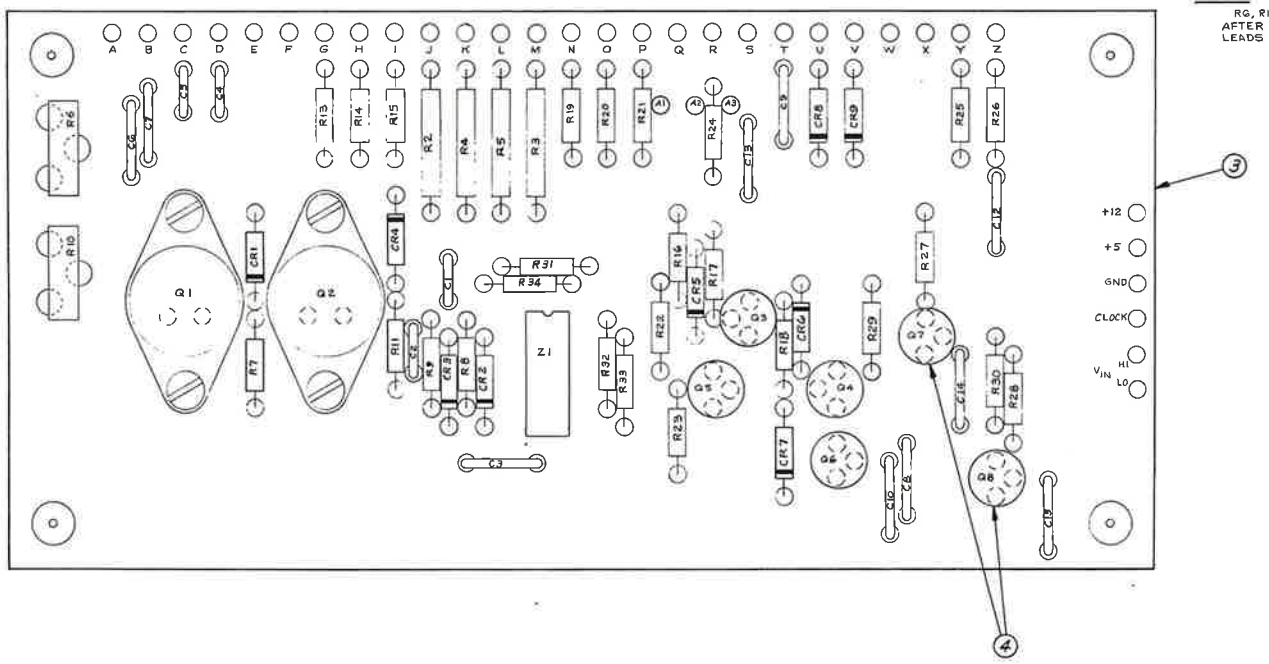
0050-434000	999	SCHEMATIC, POWER SUPPLY MODEL 999	D 020-435931 A
APPLICATION		Beckman INSTRUMENTS, INC. ELECTRONIC INSTRUMENTS DIVISION	

DR	CHK	DESCRIPTION	DATE	APP'D
	B	FINAL RELEASE		



NOTE:

RG, R10, Q1 & Q2 TO BE INSTALLED & SOLDERED AFTER WAVE SOLDERING. CLIP TRANSISTOR LEADS AFTER SOLDERING.



D 855-435940 REV B

ITEM	PART NO.	DESCRIPTION	QTY
2	D020-435941	SCHEMATIC, CONTROL	REF
1	AC27-435941	PARTS LIST, CONTROL	1

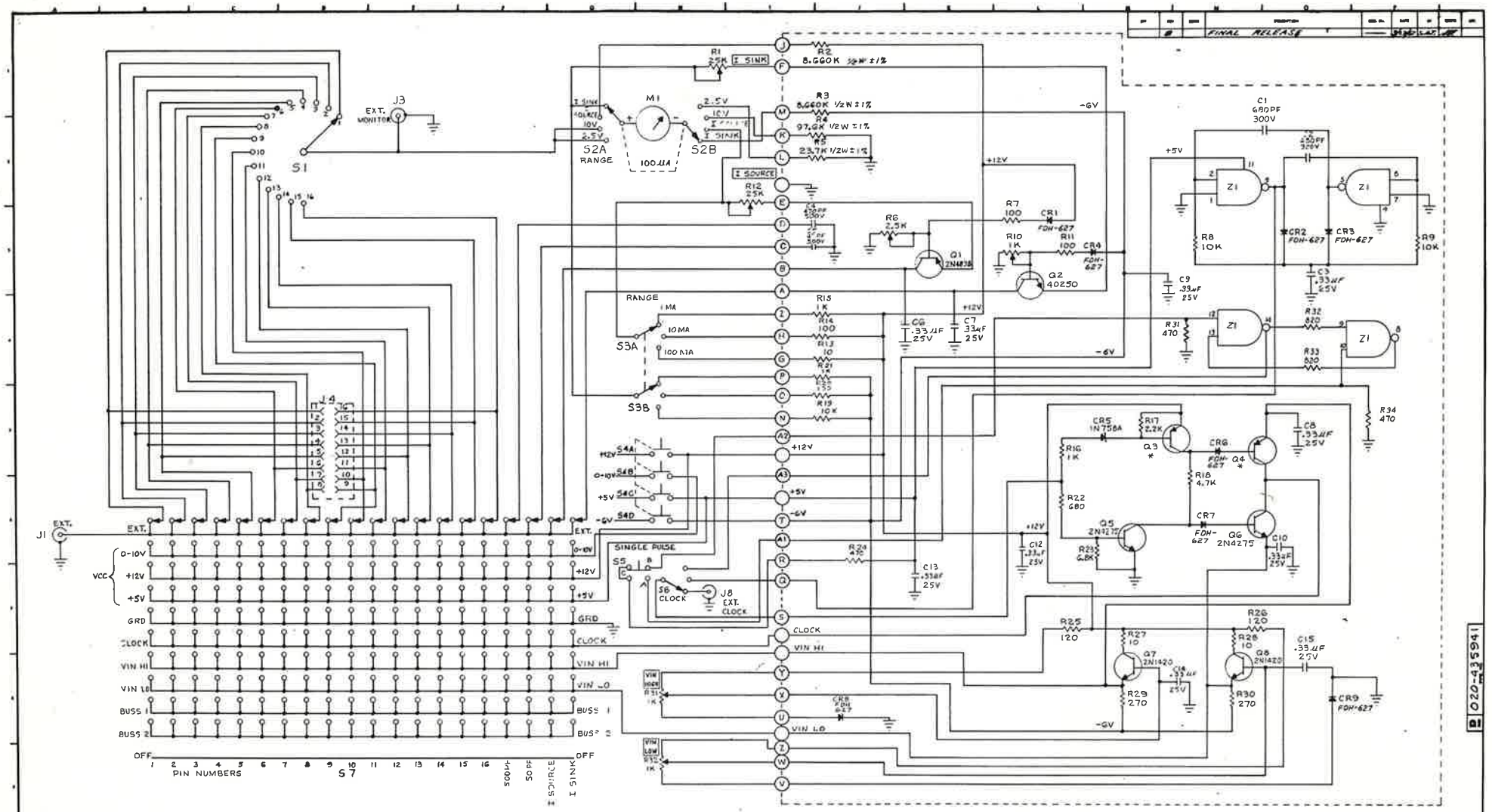
A855-435807	999
NEXT ASSY	USED ON
APPLICATION	

CONTROL BOARD ASSEMBLY
MODEL 999

Beckman INSTRUMENTS, INC.
ELECTRONIC INSTRUMENTS DIVISION

SIZE D | 855-435940 B

SCALE 3:1



NOTE:

UNLESS OTHERWISE SPECIFIED:

1. RESISTORS:
   1/4 W, 5 %
2. TRANSISTOR:
   * - ARE BECKMAN SPEC. A755-425735

B		FINAL RELEASE	

0050-426002	999
APPLICATION	

SCHEMATIC, CONTROL
MODEL 999

Beckman INSTRUMENTS, INC.
ELECTRONIC INSTRUMENTS DIVISION

D 020-435941 B

B 020-435941

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